Bhoj Reddy Engineering College for Women: Hyderabad
Department of Electronics and Communication Engineering
Lesson plan of faculty member for the academic year 2020–21

Class: III B Tech Branch-Section: ECE-A Semester: I
Subject: VLSI Design Lectures per week: 4

Lecture Number	Topics to be covered	Date (s)
	UNIT-I INTRODUCTION	
1.	Introduction: Introduction to IC Technology – MOS	2 September 2020
2.	Introduction: Introduction to IC Technology – MOS	3 September 2020
3.	Introduction: Introduction to IC Technology – PMOS	4 September 2020
4.	Introduction: Introduction to IC Technology – NMOS	5 September 2020
5.	Introduction to IC Technology-CMOS	9 September 2020
6.	Fabrication of CMOS devices	10 September 2020
7.	Fabrication of CMOS devices	11 September 2020
8.	Fabrication of BICMOS devices	12 September 2020
9.	Oxidation, Lithography, Diffusion	16September 2020
10.	Ion Implantation, Metallization, encapsulation	17 September 2020
11.	Basic Electrical Properties of MOS and BiCMOS circuits: Ids-Vds relationship	18 September 2020
12.	MOS transistor threshold Voltage	19 September 2020
13.	Gm, gds, figure of merit Co	23 September 2020
14.	Pass transistor NMOS Inverter	24 September 2020
15.	CMOS inverter analysis and design,	25 September 2020
16.	Bi-CMOS Inverters.	26 September 2020
	UNIT-II VLSI CIRCUIT DESIGN PROCESS	
17.	VLSI design flow	1 October 2020
18.	MOS layers	3 October 2020
19.	Stick diagrams	7 October 2020
20.	Design Rules and layout	8 October 2020
21.	Design Rules and layout	9 October 2020
22.	2 micron CMOS design rules	10 October 2020
23.	Design rules for wires, contacts layout for inverter Layout using NMOS, CMOS AND GATES	14 October 2020
24.	Design rules for wires, contacts layout for inverter Layout using NMOS, CMOS AND GATES	15 October 2020
25.	Scaling of MOS circuits	16 October 2020
	UNIT-III GATE LEVEL DESIGN	
26.	Logic gates and other complex gates	28 October 2020
27.	Switch Logic, Alternate gate circuit	29 October 2020
28.	Basic circuit Component	31 October 2020
29.	Sheet resistances	11 November 2020
30.	concept to MOS Area capacitance Units	12 November 2020
31.	Calculations delays	13 November 2020
32.	Driving large capacitive loads	18 November 2020
33.	Wiring Capacitance	19 November 2020
34.	Fan in Fan out	20 November 2020
35.	Logic gates	21 November 2020
36.	Choice of layers.	25 November 2020
	UNIT-IV DATA PATH SUB SYSTEMS	
37.	Introduction	26 November 2020
38.	Shifters,adders	27 November 2020
39.	ALUS	28 November 2020
40.	adders,ALUS	2 December 2020
41.	comparators	3 December 2020

42.	Counters,High Density Memory elements	4 December 2020
43.	ALUS High Density Memory elements , ROM	5 December 2020
44.	ROM, serial access memories	9 December 2020
45.	One detector,High Density Memory elements	10 December 2020
46.	SRAM	11 December 2020
47.	SRAM	12 December 2020
48.	DRAM, serial access memories	16 December 2020
UNIT- V PROGRAMMABLE LOGIC DEVICES		
49.	PLA	17 December 2020
50.	CPLD and FPGA	18 December 2020
51.	Standard cells	19 December 2020
52.	Standard cells ,System Level Test technique	23 December 2020
53.	parameters influencing low power design	24 December 2020
54.	Test Principles , Design Strategies for test	30 December 2020
55.	Design Strategies for test	31 December 2020
56.	Chip level test Technique, CMOS Testing and Test Principles	2 January 2021

Text Books:

1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005 Edition.
2. Neil H. E. Weste, David Harris, Ayan Banerjee, CMOS VLSI Design, 3rd E, Pearson, 2012.
3. VLSI Design: M.Michael Vai,2001,CRC Press.
4. CMOS VLSI Design – Niel H.E.Weste ,David Harris, Pearson, 2009.

Reference Books:

1. John P. Uyemura, Introduction to VLSI Circuits and Systems, John Wiley & sons, INC, 2002.
2. Modern VLSI Design: Wayne Wolf ,Pearson Education,1997,3rd edition.
3. K. Lal Kishore,V.S.V. Prabhakar,VLSI Design,IK International publishing house, 2013.

Name and signature of the faculty: Ms Radhika Rayeekanti ----

Name and signature of Head of the Department: Ms N Shribala ----